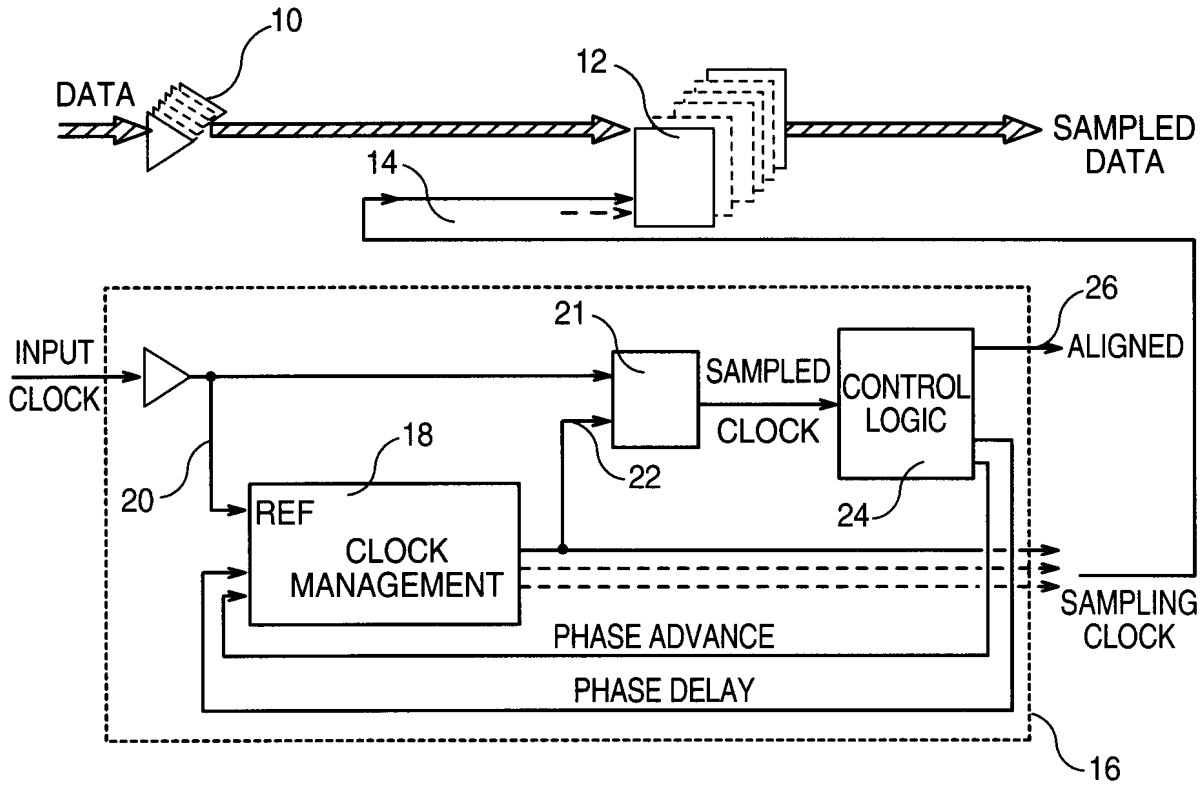

FIG. 1
PRIOR ART

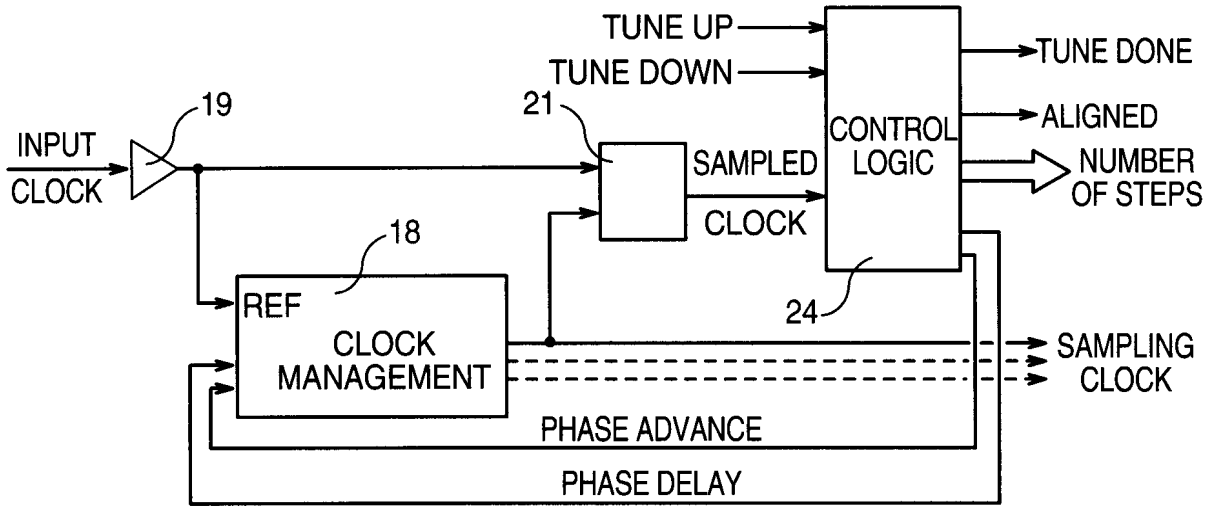

FIG. 2

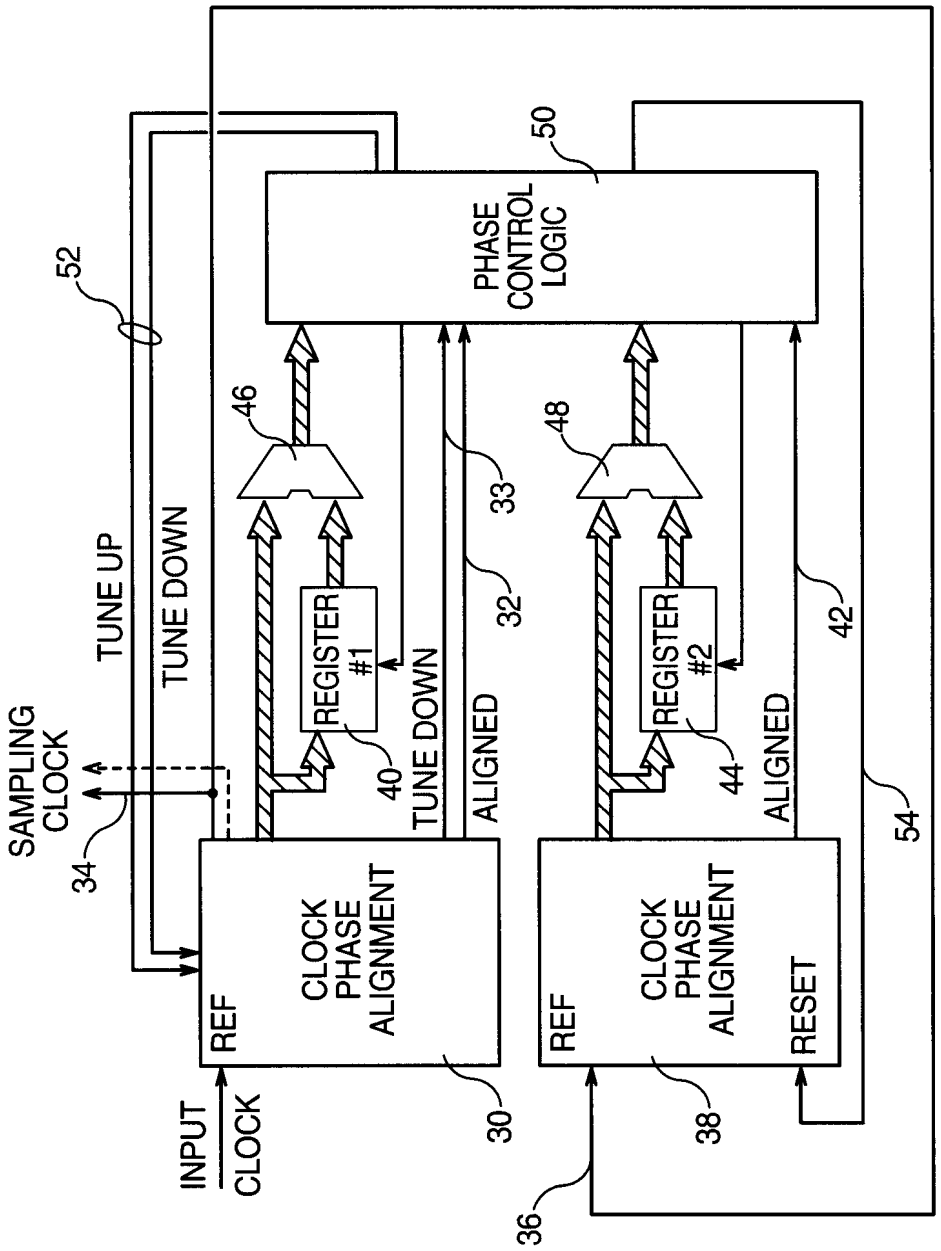
INPUT CLOCK
SAMPLING CLOCK
TUNE UP
TUNE DOWN
REF
CLOCK PHASE ALIGNMENT
REGISTER #1
REGISTER #2
PHASE CONTROL LOGIC
RESET
ALIGNED
TUNE DOWN
ALIGNED
30
32
33
34
36
38
40
42
44
46
48
50
52
54

FIG. 3

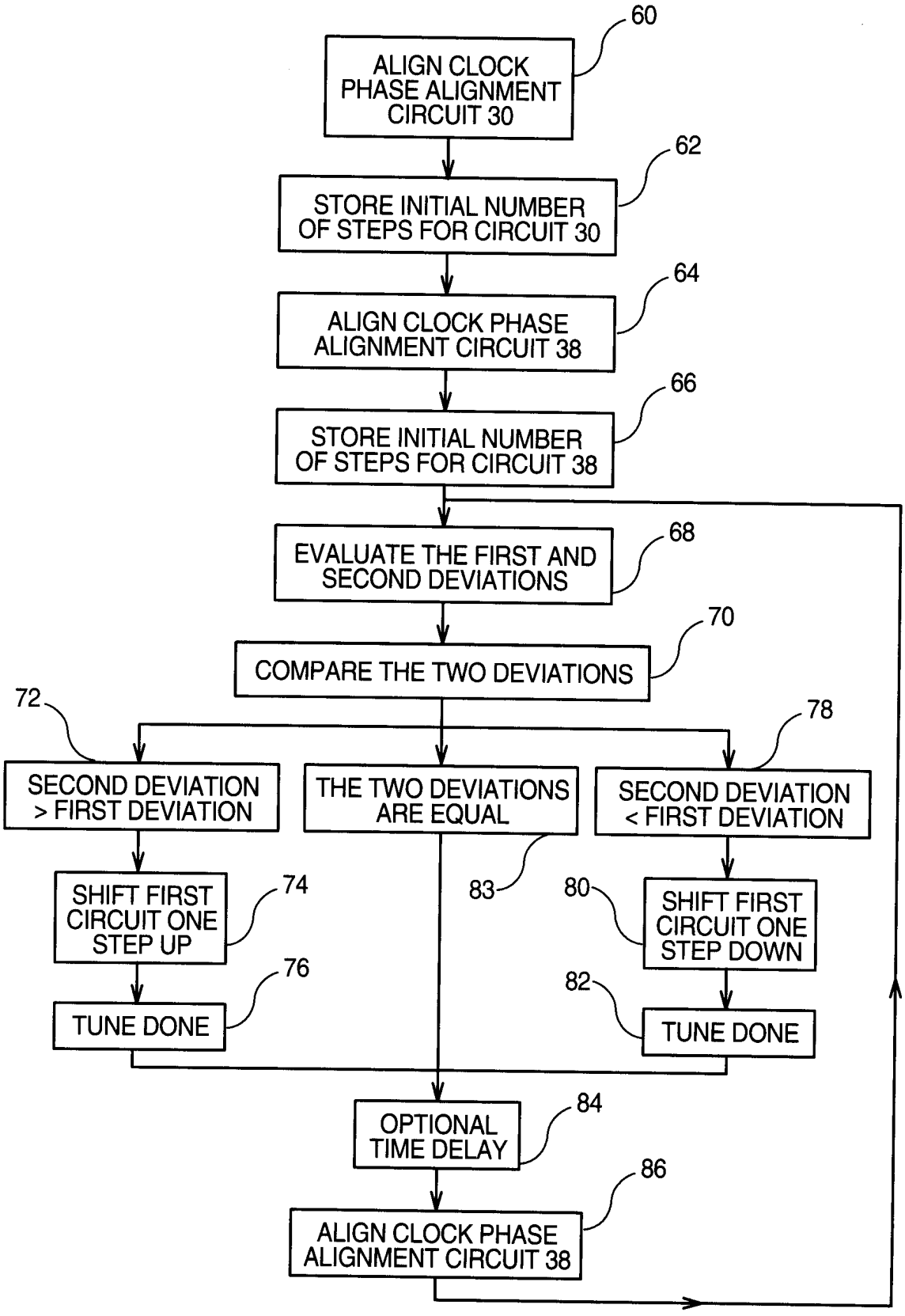
ALIGN CLOCK PHASE ALIGNMENT CIRCUIT 30
60
STORE INITIAL NUMBER OF STEPS FOR CIRCUIT 30
62
ALIGN CLOCK PHASE ALIGNMENT CIRCUIT 38
64
STORE INITIAL NUMBER OF STEPS FOR CIRCUIT 38
66
EVALUATE THE FIRST AND SECOND DEVIATIONS
68
COMPARE THE TWO DEVIATIONS
70
72
SECOND DEVIATION > FIRST DEVIATION
THE TWO DEVIATIONS ARE EQUAL
83
78
SECOND DEVIATION < FIRST DEVIATION
SHIFT FIRST CIRCUIT ONE STEP UP
74
76
TUNE DONE
80
SHIFT FIRST CIRCUIT ONE STEP DOWN
82
TUNE DONE
OPTIONAL TIME DELAY
84
ALIGN CLOCK PHASE ALIGNMENT CIRCUIT 38
86

FIG. 4